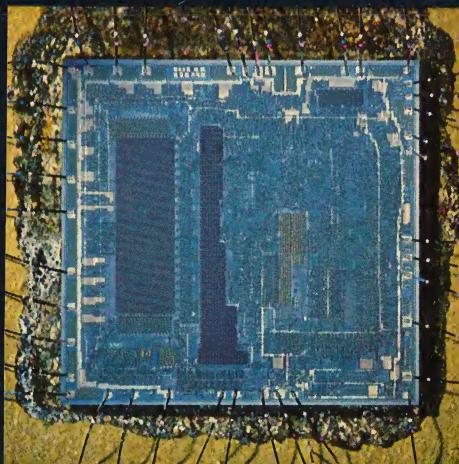


Six Steps to Success with Custom LSI

AMI

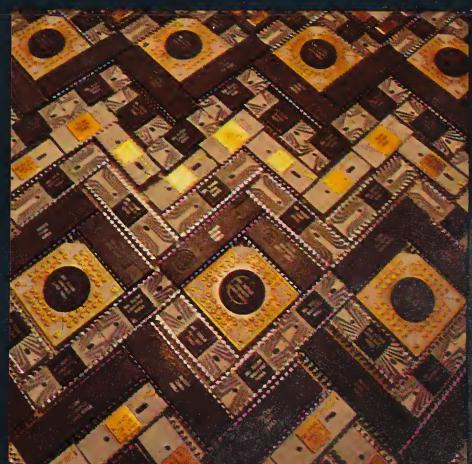




This custom circuit contains over 18,000 transistors



AMI's European Technical Center in Swindon, England



Custom circuits are packaged to the customer's needs

AMI's Six Step Program for Success in Custom LSI

If you're considering large scale integration (LSI) in the design of your product, the custom approach may be the most cost effective way to go.

Despite all the hoopla, microprocessors will not solve all your problems. Far from it, as many a manufacturer has found. For many high volume applications, a custom circuit is the most cost effective solution available—it's minimum size, minimum power and highest reliability because it's a minimum chip (often one chip) solution, tailored to your needs.

AMI has a world-wide custom LSI capability.

If the custom MOS/LSI approach seems appropriate for your particular product, and more and more customers are finding this so, you should talk to AMI, because we are acknowledged world leader in custom MOS/LSI. We're the only major high volume semiconductor company committed to the custom MOS/LSI business.

We're also the only custom circuit company with design and technology centers world wide—in Europe (at Swindon, England) and the U.S. (at Santa Clara, California and Pocatello, Idaho). Manufacturing operations are located in Santa Clara and Pocatello, while circuit assembly is done at AMI's subsidiary Korean Microsystems, Inc. (KMI) in Seoul, Korea.

No other company can match AMI's track record in developing state-of-the-art custom MOS products. With more than 1,200 custom devices designed and manufactured since 1967, AMI has more experience than any other integrated circuit company in building a wide variety of custom microcircuits.

AMI not only has the experience but the design engineering organization and the advanced production and testing facilities to produce the highest quality MOS/LSI circuits. Because AMI also offers standard memory, microprocessor, telecommunication and consumer products and the widest variety of custom LSI processes in the industry, we're able to be objective in helping customers determine their most cost effective approach.

AMI can participate at any level of the custom LSI process.

We're capable of participating at any level in the design of the

custom IC, from the classic "we'll-design-and-produce-it-for-you" approach where we have complete responsibility, to the "Customer Tooling" cooperative approach for customers who do their own design but want us to do the manufacturing. We will even enter into long-term, fully-funded joint development agreements, designing ICs for families of end products, joining together your systems designers with our circuit designers.

Since 1967, AMI has been providing customers with circuits that have enhanced the marketability of their products by adding features, increasing reliability and reducing space requirements and, finally, total systems cost.

We've developed a six step program in which you, the customer, can work with us to successfully develop the custom IC for your product by:

1. Considering All the Factors.
2. Looking At the Custom Options.
3. Selecting the Right MOS/LSI Process.
4. Designing The Best Circuit.
5. Fabricating the Optimum Device.
6. Testing For Reliable Performance.

The results are a unique product designed to your complete satisfaction.



STEP TWO: Looking at the Custom Options.

There are two basic ways AMI teams up with its customers, although we are very flexible:

- AMI designs and makes the circuit to meet customer requirements; or,
- the customer designs the IC with AMI assistance and AMI produces it.

The total AMI approach

AMI's custom capability encompasses the entire development sequence of a product. The services we provide start with five conceptual planning steps:

- System Definition;
- System Design and Partitioning;
- Preliminary Logic Design/ Simulation;
- Final Logic Design; and
- LSI Circuit Design.

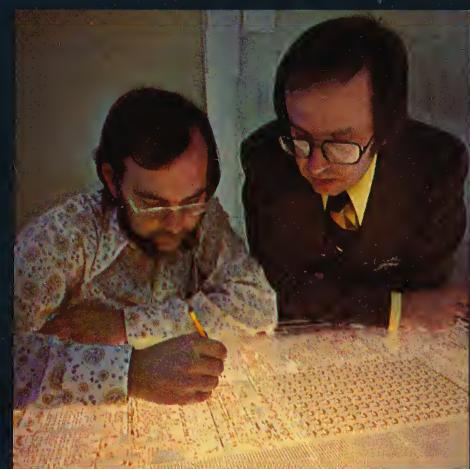
First, system definition requires the customer to have full knowledge of the system requirements for the custom IC. Working

with AMI's application engineers, the two companies form a team to develop a final system which not only meets the needs, but optimizes performance and economics.

Second, system partitioning follows the joint development of system definition. This involves the cataloging of functions into MOS subfunctions, and then into chip functions. At this step the optimum MOS process for the application is chosen. Usually, functional flow charts and timing diagrams are generated at this time as a preliminary step in logic design.

Once partitioning is complete, preliminary logic design and simulation can be done. The chip functions are translated into MOS logic diagrams. Traditional breadboarding techniques are quite often used to verify these logic designs. AMI uses proprietary computerized simulation programs for verification. These programs check the design as well as help reduce time and cost factors for design verification.

Final logic design is next. First, system errors discovered through breadboarding or simulation are corrected. Earlier partitioning may be refined if the final logic design indicates the need. During the final logic design step all system design objectives are analyzed again. MOS logic diagrams are finalized, the chip sizes are estimated, and testing procedures are generated.



Successful custom assignments flourish as cooperative enterprises

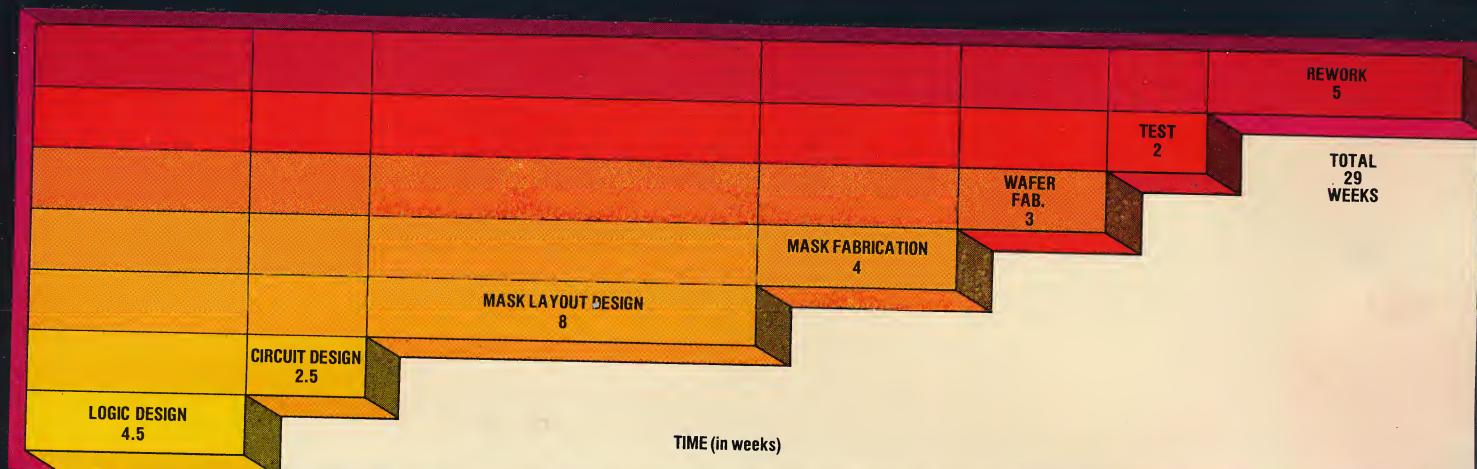
And then—the chip design. The topological chip layout is a precise science. The exact dimensions and placement for each transistor and other components must be determined. Here again AMI uses computerized circuit analysis programs to validate chip designs and verify that the design meets the performance objectives. The computerized analysis not only substantiates logic, it is an integral part of the on-going quality assurance program at AMI.

The cooperative approach

In this approach, the customer designs the circuit and has complete control over the logic and electrical requirements, the design budget and schedule, and the design changes prior to tooling.

Design workshops, consultation and information documentation packages are provided by us depending on the needs of the customer. We divide our customer interfacing into four phases: Phase 1 is a feasibility study; Phase 2 is a preliminary wafer fabrication or sample run; Phase 3, pre-production yield evaluation; and Phase 4, production.

Phase 1 begins before MOS logic is drawn. AMI customer tooling engineers provide suggestions on MOS design, discuss process and design rule parameters, provide a standard device, help plan ahead for testing, and provide information



Design span for the development of a typical custom circuit

on packaging and tooling interface.

Our experience has shown that the customer tooling interface works best when the customer is aware from the start of how we will make the device. If it's already been designed, Phase 1 begins when AMI provides a process and design rule questionnaire. This gives us information about packaging requirements, testing needs and tooling interface level. Our customer tooling experts review the data to see if AMI can meet all the requirements. At the end we supply at no charge a program plan, a firm quotation for the next two phases, and a budgetary quote for production.

During Phase 2 we'll process one wafer lot and then map, optically inspect, package and ship sample quantities of untested ICs, and, if the customer requires them, several untested wafers. Furthermore, AMI guarantees these samples will be within the agreed parameters and will meet our standards of quality and workmanship. The customer can supply working plates for Phase 2, or AMI will accept pattern generator tapes or 10x reticles.

After the customer approves the Phase 2 sample devices, AMI moves to Phase 3: pre-production yield evaluation. Here we guarantee the required manufacturing documentation, run acceptances on the test program, and build the wafer probe cards and the program board for AMI testers. We then make several

reproducibility runs of wafers and sort them for yield information.

From these runs AMI engineers will assemble and final test a number of good devices. The unit cost for them will be based on the costs of assembly, type of package and final test. These units provide the customer with a low volume production run for additional evaluation and start-up production commitments.

Pre-production deliveries actually start during Phase 3. Initial production deliveries during Phase 4 usually begin 9 to 11 weeks after approval of the pre-production units.

... But there are other options.

The custom LSI business is not an either/or sort of situation, and AMI, if nothing else, is flexible in the way we deal with our customers. The two previously described approaches are the most common ways customers themselves prefer to work with us. But AMI can interface with customers in many other ways.

For example, under certain low risk circumstances we will accept business which combines customer tooling Phases 2 and 3—prototyping and yield evaluation—prior to Phase 4 production. And for selected customers we enter into long term joint development agreements developing ICs for specific families of end products, becoming, in essence, the partner company's LSI research

and development group and production arm.

We're not biased particularly in favor of custom LSI, especially if it becomes clear it's not the best way to solve a customer problem. AMI is also a major microprocessor supplier in the 4-, 8-, and 16-bit categories: our own family of S2000 single chip microcomputers, the Motorola-designed 6800, and Texas Instrument's 9900 product line, respectively.

By having available both custom LSI and standard microprocessors, we can offer customers alternatives that can also combine the two. For example, to test the market for a new product, we can design a microprocessor-based system which provides a relatively quick, though not necessarily cost effective way to get a product to market. As part of the approach, we customize the microprocessor program or "software," and then, if the product is successful, design and make a custom LSI circuit dedicated to that particular application.

But if a microprocessor—ours or anyone else's—is the best solution, custom LSI is still useful, for microprocessors can't operate alone. They need interface devices. To achieve a system with a minimum chip count, custom devices can be designed to allow the customer to efficiently interface standard microprocessors with the customer's system.

STEP FOUR: Designing the best Circuit.



AMI interactive graphics system eliminates digitizing, allows designers to check and alter circuit design directly on computer



A key to AMI's success in the custom LSI business is its computer-aided design and layout capability. Our automated facilities are the most advanced in the semiconductor business, with a wealth of experience in supporting custom work. CAD software and hardware aids are employed at many points in the custom IC development cycle, from the early logic stage to making of the production tooling.

Logic simulation

Early in the design phase a set of computer programs is used to assure that the logic is sound. Via this simulator, the circuit's logic is modeled, exercised, and logic patterns determined for use later in test program generation. Designated the "TIDES Logic Simulator," it's especially written for MOS and contains logical functions and MOS transistors. Gate level logic simulation includes OR, AND, NOR, NAND, INVR, ROMs, shift registers, and several types of MOS transfer gates. It also includes such features as:

- multi-phase clocking schemes;
- free format input data;
- one logic element per statement;
- Boolean expressions and macros;
- user-oriented input pattern generation;
- versatile simulation and output formatting;
- convenient editing commands;
- simulation restart capability;
- input files partitioned into

constant and changeable portions; and,

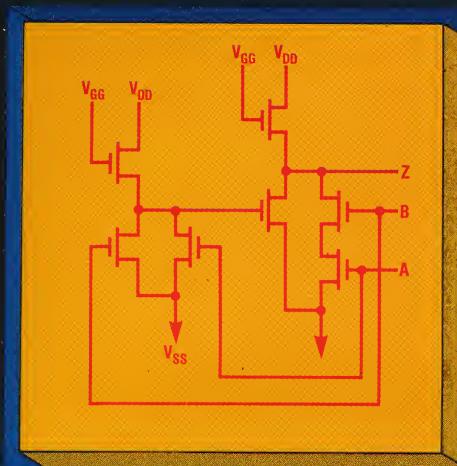
- translation of the simulation results into test patterns.

Circuit simulation

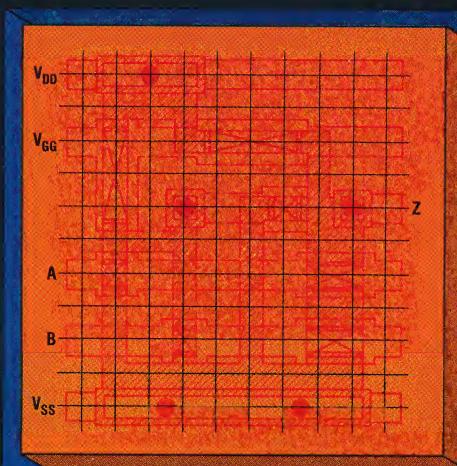
At the circuit design and topological layout phase several computer models are used to identify any potential problems, such as undesirable circuit interactions. Exactly how the circuit behaves is modeled and the results used to assure the circuit will operate with in allowable tolerances.

The ASPEC circuit simulation process allows analysis of non-linear DC, non-linear transfer functions, non-linear transients and small signal (linear) AC. Built-in component models include independent voltage and current sources; linear elements such as resistance, inductance, capacitance, transconductance, voltage controlled switches, battery and coupled-inductance; and non-linear elements such as junction field effect transistors and MOS-FETs.

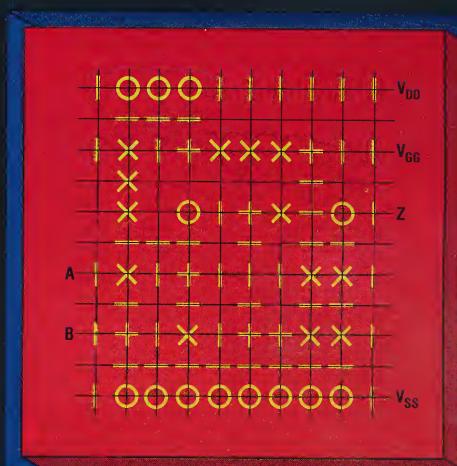
The MOS-FET modeling program allows simulation of linear and saturation region DC operation; body effect as a result of substrate bias; channel length modulation in saturation; mobility reduction at elevated gate voltages; channel pinchoff; short channel effects; weak inversion; as well as full non-linear voltage-dependent modeling of the MOS capacitors used to model transient behavior.



Circuit architecture



Topological layout



Symbolic layout (SLIC)

Symbolic layout of ICs (SLIC)

AMI has developed an advanced method of symbolic layout of MOS ICs (SLIC) that results in a reduction in the total design cycle as much as 30 to 50 percent, with half the manpower effort and at half the cost of hand-drawn approaches. The system minimizes hand-drafting by using symbols that represent complex multi-level circuit architecture. For example, an "X" stands for a transistor (see diagram in upper right), "—" for a diffusion mask, "1" for a metal mask, "0" for a contact mask, and a "+" for a metal/diffusion crossover. And as the number of masks, and therefore, the complexity of the process increases, so does the number of symbols.

The SLIC circuit layout is drawn on mylar or gridded paper in accordance with two simple rules. First, if symbols are on adjacent grids then the topologies they represent are assumed to be connected. If not, they're not connected and their separation meets or exceeds minimum mask layouts. The designer must still draw by hand, but only symbols, a much faster process than drawing the topologies. Moreover, with SLIC, the designer gets a much better feel for how the circuit is developing.

To make sure the design rules are met for the particular MOS process to be used, we have developed a sophisticated array of checking aids, including:

- SDRC, or SLIC Design Rule Checking, which checks for all symbol-to-symbol layout rule violations;
- TRACE, which traces out the symbolic layout and locates shorts between named signal lines;
- CONTINUITY, which generates a net list from the logic simulation deck and compares it to a net list from the symbolic layout and prints out any differences it finds;
- DRC, or Design Rule Checking, a set of graphical routines for manipulating and checking mask geometrical information and design rule violations. It is used for circuits not drawn and checked with SLIC.

As a result, error correction, circuit modification and area relocations take only minutes at a remote terminal connected to the control computer. This contrasts with the days for either the traditional CAD or hand-drawn approaches. The next step in time saving is currently being installed. It consists of Computer-vision interactive graphic terminal systems which permit on-line generation and editing of composite drawings.

AMI does not use so-called "computer-designed," or standard cell circuits. Our circuits are laid out by experienced designers for minimum chip size. The computer is used only as an aid. In the traditional CAD approach a computer designs a circuit by

shuffling through a library of 200 or so standard structures. The custom chips that result are usually about twice as large as those done by hand. With SLIC, custom chips are often no larger than those drawn by hand, sometimes even smaller, and at no times more than three to five percent larger.

Moreover, SLIC and the other hardware and software design aids used by AMI are process independent and can be used interchangeably with any of our processes.

HARDWARE DESIGN AIDS

- On-site Burroughs 7760 computer with multiprocessing capability.
- Computer terminals (remote job-entry and dial in, located in Santa Clara, Calif., Pocatello, Idaho, and Swindon, England) built around a Prime computer, engineering design facilities which tie in to the on-site 7760 and time-sharing services.
- Two Computervision interactive graphics systems which provide on-line generation and editing of composite drawings; includes 3 drafting surfaces and 4 CRT displays.
- 1 Calma graphics system.
- High speed, high resolution Electromask 9 track pattern generator.
- Calma GDS-II high speed electrostatic plotter.
- Calcomp 748 Flatbed Plotter.

SOFTWARE DESIGN AIDS

- Aspec Circuit Simulator
- MOSFET Model Features
- Tides Logic Simulator
 - Logic Validation
 - Pattern Validation
 - Test Word Generation
- Symbolic Layout of ICs (SLIC)
- Geometrical Design Rule Checking (DRC)
- Trace and Continuity Checking

5

STEP FIVE: Fabricating the Optimum Device.

A partnership

AMI's long history of success in the custom MOS/LSI business (see chart upper right) is the result of a close, working partnership between AMI and each of our customers.

These customers have taken advantage of orders of magnitude increases in circuit complexity over the years, thereby reducing even further the component count in their systems.

The flexibility of AMI's development program allows the customer to select the interface point which is best suited to his particular needs. The most common interface points are noted as (*) in the review of the sequence of steps involved in developing a custom MOS/LSI circuit below:

1. System Definition/Design (*)

AMI and the customer work as a team to define system parameters. This teamwork assures that the final system definition will meet the customer's requirements and use MOS to best advantage for economy and performance. This includes selecting the MOS/LSI process which best fits the application. Flow charts and timing diagrams are often generated to detail system operation.

2. Preliminary logic design and simulation (*)

Designated chip functions are then translated into a detailed MOS/LSI logic diagram. A breadboard and/or AMI's proprietary logic simulation programs are used to verify this preliminary logic design.

3. Final logic design and system design review

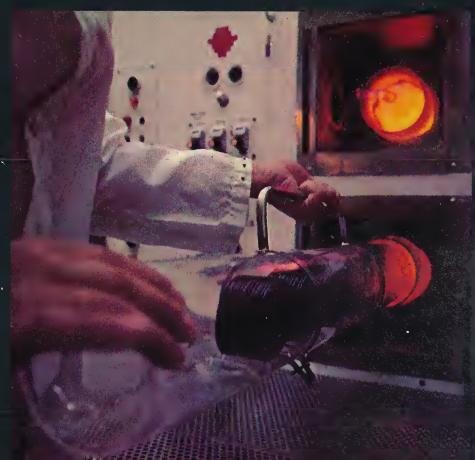
Finalization of the logic design begins by correcting any errors found during the breadboard and simulation phase. At this point the system design objectives are carefully reviewed by the customer/AMI team, the logic diagrams are finalized, chip sizes are estimated and a test word sequence is generated. Electrical specifications are also finalized in anticipation of chip circuit design.



Custom circuit replaces breadboard: 1,000 components, 2,000 feet of wire



Digitizing enters circuit design elements into the computer



Silicon wafers are baked in 1,000°C diffusion oven to help form transistors

4. Chip circuit design

In designing the topological layout of the chip, the exact size of each transistor on the final logic diagram is determined. Computerized circuit analysis techniques are used to validate the chip circuit design, verifying that it meets all of the performance objectives.

5. Topological design

The first consideration in developing the topology or "surface geography" of the integrated circuit is the design of custom MOS/LSI circuit elements or "transistors." AMI does not rely on a library of standard MOS cells. Usually, each circuit element is hand-tailored to minimize the silicon area required. With a digitizing plotter, the circuit elements are woven into a multi-level composite plot and a careful design check is again made.

6. Artwork generation (*)

At AMI, MOS/LSI artwork is predominately created by a pattern generator. Operating under computer control, this system produces a very precise reticle plate which is ten times the size of the final device. The pattern generator eliminates the cutting, stripping and first reduction steps and related problems that are commonly associated with rubylith artwork. In addition, it provides a much higher precision and tolerances.

7. Mask fabrication (*)

The 10x reticle plate is then photoreduced to the actual size of the device, and this image is duplicated anywhere from 50 to 1,000 times (depending on the chip size) onto a tooling plate. This master plate is used for creating the photomasks used for actual wafer processing.

8. Wafer fabrication and map test

After each photomask image is transferred onto photo-sensitized 3 inch wafers of silicon, a series of chemical processes impart to the wafer the properties necessary to form transistors and diffused interconnections. Fabrication is completed by depositing an aluminum layer, etching this layer to form interconnections, and then depositing a passivating glass layer. The wafer is then map tested to insure that the basic process parameters have been satisfied.

9. Wafer sort test (*)

The wafer is now electrically probed to determine which chips meet certain functional requirements. As probe testing is performed, the circuits that do not function properly are inked for future identification and separation from properly functioning circuits.

10. Packaging

The tested wafer is scribed, then broken into individual chips and 100% optically inspected. Each functionally good die is mounted in its final package. The input and output pads on the chip are connected to the lead frame with either aluminum or gold wire, followed by a 100% preseal optical inspection. The die attach cavity is flushed with dry gas and a lid is hermetically attached over the chip compartment, or the lead frame and die are totally encapsulated in plastic.

11. Final test and characterization

Packaging prototypes are now subjected to rigorous parametric and functional tests to fully validate performance per the customer's requirements.

12. Product assurance tests

AMI holds an unmatched reliability record for MOS/LSI devices because of the frequent design and manufacturing checks made throughout the custom development cycle. These frequent checks culminate when the final package is subjected to visual, electrical and dimensional tests.



offers you, through TIDS, the latest technical information on its products, check only those categories which interest you, and which are listed on the return postcard below.

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ALTHOUGH YOU MAY ALREADY BE A MEMBER OF THE TIDS SYSTEM, PLEASE COMPLETE THIS CARD TO MAKE SURE THAT ONLY YOUR CURRENT INTERESTS ARE REPRESENTED. EVEN IF YOU DO NOT WISH TO RECEIVE OTHER MANUFACTURER'S INFORMATION, MAKE SURE THAT YOU COMPLETE THE BLUE PORTION OF THE CARD AND RETURN IT TO AMI. WE WILL BE DISTRIBUTING ALL OF OUR LITERATURE ONLY THROUGH TIDS.

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3. Design Engineering (Circuits, Systems)

4. Reliability, Q-C., Test Engineer

5. Manufacturing/Production

6. R&D

7. Purchasing/Procurement

8. Marketing

9. Sales Rep or Distributor

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66. Microfiche, Reed
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72. Multimeters
73. Nucleus
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75. Oscilloscopes
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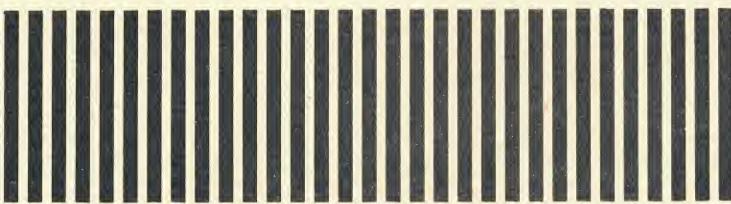
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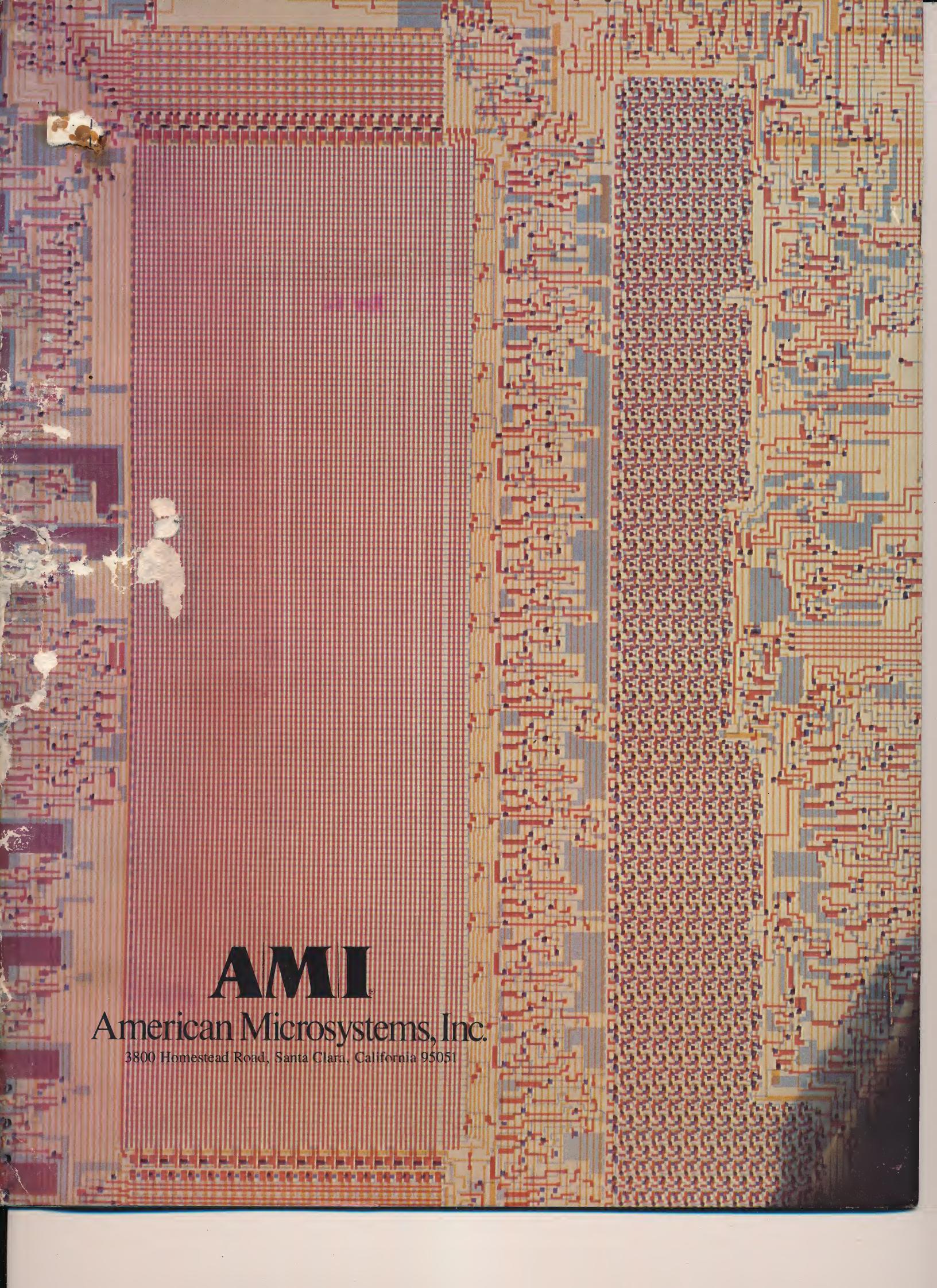
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